CERTIFICATION

I, Hiroyuki MORI of FUSOH PATENT FIRM, Rindo-building, 37, Kanda-Higashimatsushita-cho, Chiyoda-ku, Tokyo, Japan, hereby certify that I am the translator of the accompanying certified official copy of the patent application No.2000-171594 filed in Japan on the 8th day of June, 2000, and certify that the following is a true and correct translation to the best of my knowledge and belief.

Dated this 28th day of July, 2006

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Date of Application	June 8, 2000
Application Number	2000-171594
Applicant(s)	NEC Corporation

March 23, 2001

Commissioner, Patent Office Kozo OIKAWA

Certificate Number Patent-2001-3021795

[NAME OF DOCUMENT] APPLICATION FOR PATENT

[SERIAL NO.] 75310440

[DATE OF FILING] June 8, 2000

[ADDRESSEE] Commissioner, Patent Office

[INTERNATIONAL PATENT CLASSIFICATION] H01L 27/148

[TITLE OF THE INVENTION] Semiconductor Device and Method for Fabricating Same

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[PREPAYMENT NUMBER] 007009

[AMOUNT OF PAYMENT] 21000

[LIST OF DOCUMENTS ATTACHED]

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[PROOF] REQUESTED

[Document Name] Specification

[Title of Invention] SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING SAME

[Claims]

[Claim 1]

A semiconductor device comprising:

a plurality of electrode terminals arranged and formed on a mounting member; and

interconnect pads connected to the electrode terminals and formed on a substrate mounting the mounting member,

the electrode terminals forming a plurality of I/O cells each having part of the electrode terminals, the part of electrode terminals including signal terminals, the I/O cells forming a plurality of groups disposed on an inner position and an outer position of the mounting member

[Claim 2]

The semiconductor device as defined in claim 1, wherein the semiconductor member is a semiconductor chip, the electrode terminals are internal electrodes disposed on a bottom surface of the semiconductor chip, and the substrate is a package substrate used for packaging thereon the semiconductor chip.

[Claim 3]

The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package mounting a semiconductor

chip on a packaging substrate, the electrode terminals are ball electrodes for mounting arranged on a bottom surface of the packaging substrate, and the substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon.

[Claim 4]

The semiconductor device as defined in claim 1, wherein the I/O cell includes only the electrode terminals for signals or the electrode terminals for signals, power and ground intermingled among one another.

[Claim 5]

The semiconductor device as defined in claim 4, wherein the I/O cell includes peripherals.

[Claim 6]

The semiconductor device as defined in any one of claims 1 to 5, wherein an interconnect line is connected to the interconnect pad, and the interconnect lines connected to the interconnect pad of the at least one of the I/O cells are formed in a single interconnect layer.

[Claim 7]

The semiconductor device as defined in claim 6, wherein the substrate includes the interconnect pad and the interconnect line electrically connected to the interconnect pad in the single interconnect layer formed on the surface of the substrate.

[Claim 8]

The semiconductor device as defined in claim 7, wherein the interconnect lines connected to the I/O cells located on inner positions extend between the I/O cells located on the outer periphery.

[Claim 9]

The semiconductor device as defined in claim 6, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate.

[Claim 10]

The semiconductor device as defined in claim 9, wherein the I/O cells are divided into first I/O cells externally located and second I/O cells internally located, and at least one of the first I/O cells and the second I/O cells includes an outer group disposed on the outer position of the mounting member and an inner group disposed on the inner position of the mounting member

[Claim 11]

The semiconductor device as defined in claim 10, wherein the interconnect lines connected to the interconnect pads corresponding to the first I/O cells and the interconnect lines connected to the interconnect pads corresponding to the second I/O cells are formed in different interconnect layers.

[Claim 12]

A method for fabricating a semiconductor device having a plurality of electrode terminals arranged and formed on a mounting member, and interconnect pads connected to the electrode terminals and formed on a substrate mounting the mounting member comprising the steps of:

configuring the electrode terminals as a plurality of I/O cells grouped into a plurality of the electrode terminals including at lease an electrode

terminal for signals during formation and arrangement of the electrode terminals on the mounting member; and

arranging part of the I/O cells on outside of the mounting member and the other I/O cells on inner part of the mounting member with respect to the part of the I/O cells.

[Claim 13]

The method for fabricating a semiconductor device as claimed in claim 12, wherein when the I/O cell cannot be arranged after the part of the I/O cells are arranged on the outer part of the mounting member, the unarranged I/O cell is arranged on the inner part of the mounting member.

[Detailed Description of Invention]

[0001]

[Technical Field to Which Invention Pertains]

The present invention relates to an area-array semiconductor device having arranged external electrode terminals on the bottom surface of a chip or the bottom surface of a package, and more in detail to the semiconductor device having a reduced size of the chip or the package and the increased number of the external electrode terminals, and a method for fabricating the same.

[0002]

[Prior Art]

With the higher integration of a semiconductor device, the number of internal electrode terminals for externally connecting a chip or of external

electrode terminals for externally and electrically connecting a package mounting the chip is increased. On the other hand, the miniaturization of the chip or the package is advanced to reduce the size of the pitch between the terminals of internal electrodes. Accordingly, the pitch of the interconnect pads formed on a packaging substrate during the configuration of the package by mounting the chip on the packaging substrate, or the pitch of the interconnect pads formed on a mounting board for mounting the package is also reduced, and the reduced pitch makes it difficult to arrange the interconnects on the packaging substrate or mounting board. As a result, the miniaturization of the chip and the package is hardly realized.

[0003]

A semiconductor device 101 as shown in Fig.11 is an example of forming internal electrode terminals on the bottom surface of a chip which is mounted on a packaging substrate. The chip 103 has on its bottom surface a plenty of ball electrodes 131 acting as external electrode terminals arranged in a BGA (ball grid array) arrangement. The packaging substrate 102 includes, on the top surface thereof, interconnect pads 121 corresponding to the ball electrodes 131 of the chip 103 and interconnect lines 122 for connecting the respective interconnect pads 121. On the bottom surface of the packaging substrate 102 are arranged packaging ball electrodes 124 connected to the interconnect pads 121 and the interconnect lines 122 through intermediary of via-plugs 123. The chip 103 is mounted over the packaging substrate 102 and covered and sealed with resin 105, and the ball electrodes 131 of the chip 103 are connected to the interconnect pads 121 by

soldering. The semiconductor device 101 is mounted on a substrate 104, and the packaging ball electrodes 124 are connected to interconnects pads 141 formed on the top surface of the substrate 104.

[0004]

Fig.12 is schematic diagram showing the interconnect state of the interconnect pads 121 arranged on the packaging substrate 102 surface. The interconnect state of the interconnect pads 121 is substantially identical with the arrangement of the ball electrodes 131 formed on the bottom surface of the chip 103. The conventional interconnect pad arrangement has so-called peripherals including a signal line terminal (S-terminal), a power source terminal (V-terminal) and a ground terminal (G-terminal) arranged on a single line and disposed in a region corresponding to the outer peripheral of the chip 103. As shown in a partially enlarged view in Fig.12, the respective interconnect pads 121 including the S-terminal, the V-terminal and the G-terminal are arranged in the shape of a lattice by keeping specified intervals. Each of interconnect lines 122 is connected to each of the interconnect pads 121, and extends toward the outer region of the chip. The interconnect lines 122 connected to the interconnect pads 121 existing in the inner part outwardly extend between the interconnect pads 121 existing in the outer part, and the front end of the interconnect line 122 is electrically connected to the packaging ball electrodes 124 on the bottom surface of the packaging substrate 102 through intermediary of the via-plugs 123 as shown in Fig.9.

[0005]

However, in the arrangement of the above interconnect pads, due to the density of the interconnect pads 121 and the interconnect lines 122 as shown in Fig.13, the number of the interconnect lines 122 extending from the inner interconnect pads 121 is restricted because the diameter of the interconnect pad 121 is generally larger than the width of the interconnect lines 122 and the interval of the adjacent lines. When the interconnect pads 121 having a diameter of 100μm are arranged at a pitch of 250μm in Fig.13, only two interconnect lines 122 can be drawn when the line width of the interconnect lines 122 is 30μm and the line interval is 30 μm. In other words, only 12 interconnect lines 122 can be arranged in an area having a width of 1 mm in the above structure of the interconnect pads 121, and the density of the interconnect lines is 12 lines/mm. When the number of the interconnect pads is increased to increase the number of the interconnect lines, the pitch of the interconnect pads is required to be larger than 250μm as described above or the chip size is required to be larger, thereby hardly realizing the miniaturization of the chip and the packaging substrate because the larger area is necessary to arrange the interconnect pads.

[0006]

In order to solve such a problem, JP-A-10(1998)-116859 describes a technique in which interconnects pads for a standard power and a standard current which do not receive nor supply signals are disposed inside a package (chip) and the interconnects pads are connected to external connecting terminals just below the chip. In the configuration, since the

interconnect pad which does not receive nor supply signals is not required to be connected to the interconnect line, the interconnect line to be arranged among the interconnect pads is unnecessary, thereby reducing the interval between the adjacent interconnect pads. As a result, the number of the interconnect pads can be increased and the miniaturization of the chip can be attained.

[0007]

JP-A-9(1997)-69568 describes a technique in which an input-output buffer is disposed in an open region occurring in an inner circuit block-disposing area by not distinguishing an input-output buffer disposing area from the inner circuit block-disposing area in order to realize the configuration which effectively utilizes the open area occurring in the inner circuit blocks without deteriorating the fundamental algorism of a tool for automatically disposing interconnects when the input-output buffer and the inner circuit block are disposed on the chip. When the technique is applied on the chip or the package which is a subject of the present invention, at least the freedom of the disposition with respect to the disposition of the interconnect pads is elevated to effectively implement the miniaturization.

[0008]

[Problems to Be Solved by the Invention]

However, in the former publication (JP-A-10(1998)-116859), the number of the interconnect pads which do not receive nor supply signals is assumed not to be small. Accordingly, the technique cannot be applied when

the number of the interconnect pads of this kind is small and most part of interconnect pads are required to be connected to interconnect lines. If the technique is applied to part of the interconnect pads, the problem that the number of the interconnect lines externally drawn with respect to the interconnect pad connected to the interconnect line is restricted cannot be solved.

[0009]

In the latter publication (JP-A-9(1997)-69568), the number of the input-output buffers depends on the open area occurring among the inner circuit blocks, and when the open areas are concentrated, it is uncertain that the interconnect lines are drawn from the input-output buffers. Accordingly, the interconnect pads must be designed for every floor plan to increase a period of time (turn-around time, TAT). When the drawing-out of the interconnect lines is hardly attained, the effective means for responding thereto does not exist so that the above problem cannot be solved.

[0010]

In the above technique, the interconnect line formed on the packaging substrate is assumed to be a single layer. When the interconnect line formed on the packaging substrate is made to be a multi-layered structure having two or more layers, the structure increases the freedom of arranging the interconnect lines to assist to solve the above problem. However, the multi-layered structure may make the interconnect lines of the upper layer and the lower layer crossed with each other to hardly

perform the impedance matching among the interconnect lines, thereby affecting larger adverse effects on the semiconductor device. Accordingly, it is not preferable.

[0011]

In view of the foregoing, an object of the present invention is to provide a semiconductor device in which a chip or a package is miniaturized and the number of terminals of external connection terminals is increased, and a method for fabricating the same.

[0012]

[Means for Solving Problems]

Thus, the present invention provides a semiconductor device comprising a plurality of electrode terminals arranged and formed on a mounting member, and interconnect pads connected to the electrode terminals and formed on a substrate mounting the mounting member, the electrode terminals forming a plurality of I/O cells each having part of the electrode terminals, the part of electrode terminals including signal terminals, the I/O cells forming a plurality of groups disposed on an inner position and an outer position of the mounting member. For example, the mounting member is a semiconductor chip, the electrode terminals are internal electrodes disposed on the bottom surface of the semiconductor chip, and the substrate is a package substrate used for packaging thereon the semiconductor chip. Or the mounting member is a semiconductor package mounting a semiconductor chip, the electrode terminals are ball electrodes

for mounting arranged on the bottom surface of the packaging substrate, and the substrate is the mounting substrate for forming a specified circuit by mounting the semiconductor package thereon.

[0013]

The I/O cell may include only the electrode terminals for signals or the electrode terminals for signals, power and ground intermingled among one another. The may include peripherals.

[0014]

In accordance with the present invention, the higher integration of the semiconductor device having the higher performances can be realized because the interconnect lines can be drawn to the outer periphery of the chip from the interconnect pads corresponding to each of the I/O cells when the chip is miniaturized or the number of the ball electrodes is increased by dividing the electrode terminals such as internal electrodes into the I/O cells and arranging part of the I/O cells in the position of the outer periphery of the mounting member such as the chip and arranging the other I/O cells in the position of the inner periphery thereof.

[0015]

The interconnect line is connected to the interconnect pad in the substrate, and the interconnect lines connected to the interconnect pad of the at least one of the I/O cells are formed in a single interconnect layer. That is, the substrate includes the interconnect pad and the interconnect

line electrically connected to the interconnect pad in the single interconnect layer formed on the surface of the substrate. In this case, the interconnect lines connected to the I/O cells located on inner positions extend between the I/O cells located on the outer periphery. The interconnect pads and the interconnect lines electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate. In this case, the I/O cells are divided into first I/O cells externally located and second I/O cells internally located, and at least one of the first I/O cells and the second I/O cells includes an outer group disposed on the outer position of the mounting member and an inner group disposed on the inner position of the mounting member. The interconnect lines connected to the interconnect pads corresponding to the first I/O cells and the interconnect lines connected to the interconnect pads corresponding to the second I/O cells are formed in different interconnect layers.

[0016]

Since the interconnect pads and the interconnect lines corresponding to the I/O cell is made by the single conductive film in the present invention, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines. Especially, when the interconnect pads and the interconnect lines corresponding to the plurality of the input-output buffers are intermingled in the single I/O cell, the proper impedance matching is possible by preventing the mutual intervention between the interconnect lines of each of the input-output buffers. Since each of the corresponding

first I/O cell and the second I/O cell are arranged in the different interconnect lines, each of the I/O cells can be arranged in the inner position and the outer position even when both of the I/O cells are arranged in the outer periphery and the inner periphery of the chip. Further, the impedance matching on each of the interconnect lines corresponding each of the I/O cells can be easily performed.

[0017]

The method for fabricating the semiconductor device having the plurality of the electrode terminals arranged and formed on the mounting member, and the interconnect pads connected to the electrode terminals and formed on the substrate mounting the mounting member in accordance with the present invention characterized by including the steps of: configuring the electrode terminals as a plurality of I/O cells grouped into a plurality of the electrode terminals including at lease an electrode terminal for signals during formation and arrangement of the electrode terminals on the mounting member, and arranging part of the I/O cells on outside of the mounting member and the other I/O cells on inner part of the mounting member with respect to the part of the I/O cells. In this case, when the I/O cell cannot be arranged after the part of the I/O cells are arranged on the outer part of the mounting member, the unarranged I/O cell is arranged on the inner part of the mounting member. Thereby, the semiconductor device of the present invention can be fabricated.

[0018]

[Embodiments of the Invention]

Then, the embodiments of the present invention will be described referring to annexed drawings. Fig.1 is a vertical sectional view showing an entire semiconductor device in accordance with a first embodiment of the present invention and a partial enlarged view thereof. A semiconductor device 1 includes a packaging substrate 2 and a chip 3 mounted thereon. The packaging substrate 2 is formed by a dielectric plate material and includes, on the top surface thereof, a plenty of interconnect pads 21 and interconnect lines 22 formed by etching a conductive film made of copper. The interconnect pads 21 and the interconnect lines 22 are connected to for mounting ball electrodes 24 on the bottom surface of the packaging substrate 2 through intermediary of via-plugs 23 formed through the packaging substrate 2. A flame-like spacer 25 is fixed to the periphery of the top surface of the packaging substrate 2 by using an adhesive agent, and accommodates the chip in the region surrounded by the spacer 25. A covering plate 27 is fixed on the spacer 25 by using another adhesive agent 26 to seal the chip 3.

[0019]

The chip 3 is formed by a semiconductor substrate such as silicon, and various elements such as a transistor not shown in the drawing are formed on the bottom main surface of the chip 3 and are covered with a protective dielectric film such as a passivation film. On the surface of the protective dielectric film or on the bottom surface of the chip are formed and arranged ball electrodes 31 made of solder, connected to the above elements, acting as

internal electrodes. The ball electrodes 31 are soldered to the interconnect pads 21 formed on the packaging substrate 2 to mount the chip 3 on the packaging substrate 2 in a face-down manner, and the elements in the chip 3 are electrically connected to the ball electrodes 24 on the bottom surface of the packaging substrate 2 through intermediary of the ball electrodes 31 and the interconnect pads 21. The chip 3 is sealed is sealing resin 28.

[0020]

In this embodiment, the semiconductor device 1 is mounted on a mounting substrate 4. A specified interconnect pattern is formed on a dielectric substrate by using a conductive film to prepare the mounting substrate 41. The interconnect pattern includes interconnects pads 41 connected to the ball electrodes 24 of the semiconductor device 1 and interconnect lines, not shown in the drawings, for connecting the interconnect pads 41 among one another on the mounting substrate 4 or the interconnect pad 41 with interconnect lines not shown in the drawings for connecting the interconnect pad 41 to an external circuit.

[0021]

An example of configuration will be described in which the ball electrodes 31 are formed and arranged on the bottom surface of the chip 3 of the semiconductor device 1 and interconnect pads 21 are formed and arranged on the top surface of the packaging substrate 2 corresponding to the ball electrodes 31. Fig.2 is a schematic view showing interconnect pads 21 arranged on a packaging substrate 2, this arrangement corresponds to

the ball electrodes 31 arranged on the bottom surface of the chip 3. The ball electrodes 31 on the bottom surface of the chip 3 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in the same drawing in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The I/O cell is, for example, a single group including a single unit having one or more input-output buffers formed in the chip 3 and an S-terminal (signal line terminal), a V-terminal (power source terminal) and a G-terminal (ground terminal) connected to the input-output buffers, or the single I/O cell may include only the S-terminal. However, the number of the terminals and the arrangement are not restricted to the above, and an I/O cell having an arbitrary array can be formed.

[0022]

Among the grouped I/O cells, part of the I/O cells (CELL-A) are disposed on the periphery of the chip 3 similarly to the conventional chip, and the remaining cells (CELL-B) are internally disposed from the above I/O cells (CELL-A) at a specified interval. In this case, the adjacent I/O cells (CELL-A) disposed on the periphery have a specified space therebetween. In this embodiment, if the additional space exists between the adjacent I/O cells (CELL-A), peripherals (PL) conventionally used are also disposed. That

is, the peripherals intermingle in a space where the interconnect pads 21 do not have an array of 4 x 3.

[0023]

Fig.3 is an partially enlarged view showing the interconnect pads 21 formed on the top surface of the packaging substrate 2, and interconnect lines 22 connected these interconnect pads 21. In the drawing, two outer peripheral I/O cells (CELL-A) on the chip 3 are disposed with a specified interval along the periphery, and one inner I/O cell (CELL-B) is disposed in a space opposing to the location between the two outer peripheral I/O cells (CELL-A). Similarly to the preceding example, the interconnect lines 22a are connected to each of the interconnect pads 21a of the two outer peripheral I/O cells (CELL-A), and are drawn between the interconnect pads 21a to regions external to the chip 3. On the other hand, the interconnect lines 22b are connected to each of the interconnect pads 21b of the inner peripheral I/O cell (CELL-B), and are drawn similarly to the preceding example in the region of the peripheral I/O cell (CELL-B), and are bundled at a specified interval, at a region out of the inner peripheral I/O cell (CELL-B), to be drawn between the outer peripheral I/O cells (CELL-A) to regions external to the chip 3.

[0024]

In the structure of the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 2, the density of arranging the interconnect lines 21a at the I/O cells (CELL-A) arranged on the outer periphery of the

chip 3 is substantially the same as the density of the conventional device shown in Fig.13. However, the density of arranging the interconnect lines 21b connected to the interconnect pad 21b of the I/O cells (CELL-B) arranged inside of the chip 3 can be increased because of the absence of the interconnect pads. When the line width of the interconnect lines connected to the 12 interconnect pads 21 is 30μm and the line interval is 30μm as shown in Fig.3, the dimension of arranging the 12 bundled interconnect lines 22i is 750μm. The number of the interconnect lines 22 in the region having a size of 2 mm along the outer periphery of the chip is 27 calculated by adding the number of the interconnect lines 22a of the outer peripheral I/O cells (CELL-A) to the number of the interconnect lines 22b of the inner I/O cells (CELL-B). The density of the interconnect lines 22 is 13.5 lines/mm in the embodiment, and is increased compared with conventional density of 12 lines/mm shown in Fig.13.

[0025]

Thereby, even when the size of the chip 3 is reduced for miniaturization or the numbers of the ball electrodes 31 and the interconnect pads 21 are increased with the chip 3 having the same size, the higher integration of the semiconductor device having the higher performances can be realized by dividing the ball electrodes 31 disposed on the chip 3 and the interconnect pads arranged on the packaging substrate 12 into the plurality of the I/O cells and disposing part of the I/O cells at the outer periphery of the chip 3 and the remaining I/O cells at the corresponding inner sections of the chip 3 because the drawing-out of the

interconnect lines 22 to the peripheral outer regions of the chip on the top surface of the packaging substrate 2 is possible. Especially, as shown in Fig.3, since the interconnect lines of the other I/O cells do not pass through the I/O cells (CELL-B) disposed on the inner section of the chip, the I/O cells (CELL-B) may be formed endlessly or annually to enable the arrangement of the extremely larger number of the ball electrodes 31 and the interconnect pads 21. An interval may exist between the I/O cells (CELL-B) disposed on the inner section. The ball electrodes 31 and the interconnect pads 21 of the outer peripheral I/O cells (CELL-A) may be freely disposed so long as the spaces through which the interconnect lines 22 of the I/O cells (CELL-B) disposed on the inner section pass may be secured, thereby promoting the higher integration of the semiconductor device having the higher performances. The I/O cells can be freely disposed in the regions of the chip 3 so long as the above requisites are satisfied to increase the freedom of the chip design and the package design.

[0026]

Since the interconnect pads 21 and the interconnect lines 22 in the embodiment are made by the conductive film having the single layer, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines. Especially, when the interconnect pads and the interconnect lines corresponding to the plurality of the input-output buffers are intermingled in the single I/O cell, the proper impedance matching is possible by preventing the mutual intervention between the interconnect

lines of each of the input-output buffers.

[0027]

Fig.4 is a vertical sectional view showing an entire semiconductor device in accordance with a second embodiment of the present invention and an enlarged view of the substantial part thereof in which the same numerals as those of the first embodiment designate the same elements. A semiconductor device 1 includes a packaging substrate 2A and a chip 3 mounted thereon in this embodiment. The packaging substrate 2A includes a central core layer 211 sandwiched between a pair of buildup layers 212, 213, and a plenty of interconnect pads 21 made of a conductive film are formed thereon. The interconnect pads 21 are connected to the interconnect lines in each of the multi-layers of the top buildup layer 212, further connected to the bottom buildup layer 213 through intermediary of via plugs 23, and still further connected to ball electrodes 24 formed on the bottom surface of the bottom buildup layer 213 or the bottom surface of the packaging substrate 2A.

[0028]

Each of the buildup layers is multi-layered, and the top buildup layer 212 includes five interconnect layers in which a first layer includes the interconnect pads 21 and a GND layer 1G, a third layer includes a GND layer 3G and a VDD layer 3V, and a fifth layer includes a GND layer 5G and a VDD layer 5V connected to the via plugs of the above core layer. A second layer and a fourth layer are formed as independent interconnect lines 22a,

22b for signals. In the second embodiment, the interconnect lines formed in the single layer in the first embodiment are divided into the first to fifth interconnect layers 201 to 205. Especially, the interconnect lines connected to the interconnect pad 21 acting as the S-terminal (signal terminal) can be drawn as the interconnect lines 22 of the second and fourth layers separately from the others.

[0029]

In view of the increased number of layers (two-layered) of the interconnect lines 22a, 22b, as schematically shown in Fig.5, the grouped I/O cell in the arrangement of the interconnect pads 21 (as well as the ball electrodes 31 of the chip 3) can be divided into a first I/O cell (CELL-1) and a second I/O cell (CELL-2). Part of the first I/O cell (CELL-1) or I/O cells (CELL-1A) are disposed on the outer peripheral region of the chip 3, and the remaining I/O cells (CELL-1B) are disposed on the inner sections thereof. Intervals are secured between the first I/O cells (CELL-1A) remaining on the outer periphery for passing the interconnect lines 22 drawn from the inner I/O cells (CELL-1B). Herein, the first I/O cells (CELL-1) disposed on the outer periphery of the chip are alternately disposed on outer sections (CELL-1A) and inner parts (CELL-1B) in the outer periphery. The second I/O cells (CELL-2) are disposed on the sections inside of the other I/O cells (CELL-1), and part of the second I/O cell (CELL-2) or I/O cells (CELL-2B) are disposed inside of the remaining I/O cells (CELL-2A) and intervals are secured between the outer second I/O cells (CELL-2A) for passing the interconnect lines drawn from the inner second I/O cells (CELL-2B). Herein,

similarly to the first I/O cells (CELL-1), the second I/O cells (CELL-2) are alternately disposed on outer sections (CELL-2A) and inner parts (CELL-2B) arranged along the circumference of the chip.

[0030]

Referring again to Fig.4, the interconnect line 22-1 connected to the interconnect pad 21-1 of the first I/O cell (CELL-1) is connected in its outer region to the second interconnect layer 202 of the top buildup layer 212 and drawn to the outer region by the second interconnect layer 202. The interconnect line 22-2 connected to the interconnect pad 21-2 of the second I/O cell (CELL-1) is connected in the area between its outer region and the first I/O cell (CELL-1) to the fourth interconnect layer 204 of the top buildup layer 212 and drawn to the outer region by the fourth interconnect layer 204. Accordingly, the interconnect line 22-2 connected to the second I/O cell (CELL-2) is never drawn to the outer region through the first I/O cells (CELL-1). The interconnect lines 202, 204 of the second and the fourth layers are connected to the via plugs 23 of the core layer 211 at specified positions and apparently further connected to the ball electrodes 24 on the bottom surface of the packaging substrate 2A through intermediary of the bottom buildup layer 213.

[0031]

The configuration of the interconnect pads 21 and the interconnect lines 22 on the top surface of the packaging substrate 12A obtained in this manner is similar to that shown in Fig.3 for each of the first I/O cell

(CELL-1) and the second I/O cell (CELL-2), and enables to elevate the density of the interconnect pads 21 and the interconnect lines 22 of the first I/O cell (CELL-1) and the second I/O cell (CELL-2) by dividing the I/O cells into the first and the second I/O cells (CELL-1 and CELL2) which are positioned in the corresponding regions of the outer periphery and the inner periphery of the chip, respectively, and further arranging each of the I/O cells separately arranged in the outer section and the inner section. Since the first I/O cell (CELL-1) and the second I/O cell (CELL-2) are double-disposed in the second embodiment, the density almost twice that of the first embodiment can be obtained. Thereby, even when the chip is miniaturized or the numbers of the ball electrodes and the interconnect pads are increased, the higher integration of the semiconductor device having the higher performances can be realized by drawing the interconnect lines of each of the I/O cells.

[0032]

Since the interconnect lines 22-1 of the first I/O cell (CELL-1) is drawn by the second interconnect layer 202 and the interconnect lines 22-2 of the second I/O cell (CELL-2) is drawn by the fourth interconnect layer 204 in the second embodiment, the interconnect lines connected to the respective I/O cells are drawn to the single interconnect layer and are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines. Especially, when the interconnect pads and the interconnect lines corresponding to the plurality of the input-output buffers are intermingled in the single I/O cell, the proper impedance matching is

possible by preventing the mutual intervention between the interconnect lines of each of the input-output buffers similarly to the first embodiment.

[0033]

The first I/O cell (CELL-1) and the second I/O cell (CELL-2) in the second embodiment can be arranged as shown in Figs.6. In Fig.6a, only for the first I/O cell (CELL-1), the outer I/O cell (CELL-1A) and the inner I/O cell (CELL-1B) are disposed. In Fig.6b, only for the second I/O cell (CELL-2), the outer I/O cell (CELL-2A) and the inner I/O cell (CELL-2B) are disposed. As shown in Fig.6c, apparently, each of the first I/O cell (CELL-1) and the second I/O cell (CELL-2) may be disposed in a single row. As shown in Fig.7, either of the first I/O cell (CELL-1) and the second I/O cell (CELL-2) is not the I/O cell but may be the conventional peripherals. In Fig.7a, the outer peripheral section is formed by peripherals PL and the inner section is formed by the second I/O cell (CELL-2). In Fig.7b the inner second I/O cell (CELL-2) of Fig.7a is formed by the outer I/O cell (CELL-2A) and the inner I/O cell (CELL-2B). In Fig.7c, the outer peripheral section is formed by the first I/O cell (CELL-1) and the inner section is formed by the peripherals PL. As shown in Fig.7d, the outer first I/O cell (CELL-1) may be formed by the outer I/O cell (CELL-1A) and the inner I/O cell (CELL-1B).

[0034]

As shown in Figs.8a to 8d corresponding to Figs.7a to 7d, respectively, part of the first I/O cell (CELL-1) or the second I/O cell (CELL-2) is formed by the peripherals PL to intermingle the I/O cells and the peripherals PL.

Similarly, as shown in Figs.9a to 9d, part of the first I/O cells (CELL-1A, CELL-1B) or the second I/O cells (CELL-2A, CELL-2B) formed by the inner I/O cells and the outer I/O cells may be formed by the peripherals PL. In either case, the higher integration of the semiconductor device having the higher performances can be realized compared with the conventional configuration as shown in Fig.12 because the ball electrodes and the number of the interconnect pads can be increased.

[0035]

The method of disposing the ball electrodes 31 and the interconnect pads 21 as the I/O cells are substantially the same for the semiconductor devices of the first and the second embodiments. The method for disposing the semiconductor device in the first embodiment will be described referring to a flow chart shown in Fig.10. At first, a template having I/O cells and peripherals to be disposed on a chip along the outer periphery of the chip is fabricated (S101). Then, the judgment is conducted whether or not the numbers of the balls electrodes and the interconnect pads of the I/O cell and the peripherals, and the number of required terminals reach to specified values (S102). When the numbers reach to the required values, the judgment is conducted whether or not the request for disposing I/O cells at the center of the chip (S103) is present. In absence of the request, the disposal is finished (S104). In present of the request for disposing the I/O cells at the center of the chip, the cell is moved in accordance with a floor plan (S105). When the movement is possible, the disposal is finished (S104). When the movement is impossible, the step (S105) is again executed after

the floor plan and the I/O cells are modified. When the movement is also impossible after the repetition of the processes, a following step (S108) is initiated.

[0036]

On the other hand, when the number of the terminals does not reach to the required number in the step (S102), the number of the I/O cells disposed on the inner sections of the chip is calculated (S107) for increasing the number to the required one. Then, another new template having a reduced interval between the I/O cells is fabricated (S108). Then, the I/O cell is moved in accordance with a floor plan (S109). When the movement of all the I/O cells is possible at this stage, the disposal is finished (S104) because the I/O cells can be disposed on the outer periphery and on the inner section of the chip. When at least one of the I/O cells cannot move, the step (S109) is again executed after a further template having a reduced interval between the I/O cells is fabricated (S110). Or, depending on necessity, the step (S109) is again executed after the modification of the floor plan and the I/O cells. When the disposal of all the I/O cells is not finished after the plurality of the re-executions, the disposal is recognized to be failed, and the procedures are started from the first step (S101) after the chip is enlarged or the number of the interconnect layers is increased.

[0037]

In the second embodiment, a process of diving the I/O cells into the first I/O cell and the second I/O cell is inserted between the steps (S107) and

(S108), and the processes are conducted on and after the step (S108) for each of the I/O cells.

[0038]

In the method described above, after the I/O cells are formed by grouping the S-terminal, the V-terminal and the G-terminal, the method of disposing the interconnect pads of the I/O cell and drawing the interconnect lines connected to the interconnect pads is determined in advance. Thereby, the propriety of drawing the interconnect lines at the time of preparing the floor plan can be easily judged to advantageously reduce TAT. The method can be easily customized for every kind of the semiconductor devices by suitably using the I/O cells having different usages after the usages of each of the I/O cells are stored as information.

[0039]

Although the array of 4 x 3 is exemplified as the arrangement of the I/O cells in the previous embodiments, the I/O cells can be arranged in an array having an arbitrary number. Depending on cases, the I/O cell may be formed by disposing the plurality of the conventional peripherals.

[0040]

Although the examples are described for applying the configuration of the present invention to the ball electrodes 31 formed on the bottom surface of the chip 3 and the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 2, 2A in the preceding embodiments as shown Figs.

1 and 4, the present invention may be also applied to the ball electrodes 24 of the semiconductor device 1 and the interconnect pads 41 and the interconnect lines on the mounting substrate 4. The ball electrodes 24 on the bottom surface of the packaging substrate 2, 2A and the interconnect pads 41 on the top surface of the mounting substrate 4 are disposed as the I/O cells to increase the density of the ball electrodes 24 and the interconnect pads 41 to achieve the miniaturization of the chip and further to increase the number of the terminals, the higher integration of the semiconductor device having the higher performances can be realized. When the configuration of the second embodiment is applied, the mounting substrate 4 is multi-layered.

[0041]

[Effect of the Invention]

As described above, in accordance with the present invention, the higher integration of the semiconductor device having the higher performances can be realized because the interconnect lines can be drawn to the outer periphery of the chip from the interconnect pads corresponding to each of the I/O cells when the chip is miniaturized or the number of the ball electrodes is increased by dividing the electrode terminals such as internal electrodes into the I/O cells and arranging part of the I/O cells in the position of the outer periphery of the mounting member such as the chip and arranging the other I/O cells in the position of the inner periphery thereof.

[0042]

Since the interconnect pads and the interconnect lines corresponding to the I/O cell is made by the single conductive film in the present invention, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines. The higher integration of the semiconductor device having the higher performances can be realized because the I/O cells are divided into the first I/O cells externally located and the second I/O cells internally located, and the I/O cells are arranged in the inner and outer positions of the chip. Since each of the corresponding first I/O cell and the second I/O cell are arranged in the different interconnect lines, each of the I/O cells can be arranged in the inner position and the outer position even when both of the I/O cells are arranged in the outer periphery and the inner periphery of the chip. Further, the impedance matching on each of the interconnect lines corresponding each of the I/O cells can be easily performed.

[Brief Description of Drawings]

[Fig.1]

A vertical sectional view showing an entire semiconductor device in accordance with a first embodiment of the present invention and a partial enlarged view thereof.

[Fig.2]

A schematic view showing arrangement of interconnect pads and interconnect lines on a packaging substrate in the first embodiment.

[Fig.3]

A schematic view showing the density of the conventional interconnect pads and interconnect lines shown in Fig.2.

[Fig.4]

A vertical sectional view showing a semiconductor device in accordance with a second embodiment of the present invention and an enlarged view thereof.

[Fig.5]

A view showing arrangement of interconnect pads and interconnect lines of a packaging substrate of the second embodiment.

[Fig.6]

A view showing first modification of the arrangement of the ball electrodes and the interconnect pads of the second embodiment.

[Fig.7]

A view showing second modification of the arrangement of the ball electrodes and the interconnect pads of the second embodiment.

[Fig.8]

A view showing third modification of the arrangement of the ball electrodes and the interconnect pads of the second embodiment.

[Fig.9]

A view showing fourth modification of the arrangement of the ball electrodes and the interconnect pads of the second embodiment.

[Fig.10]

A flowchart sequentially showing the steps of fabricating the semiconductor device of the present invention.

[Fig.11]

A sectional view showing a conventional semiconductor device.

[Fig.12]

A view showing arrangement of interconnect pads and interconnect lines of a packaging substrate of the conventional semiconductor device.

[Fig.13]

A view showing the density of arrangement of conventional interconnect pads and interconnect lines.

[Description of Symbols]

1 semiconductor device.

2, 2A packaging substrate

3 chip

4 mounting substrate

21 interconnect pad

22 interconnect line

23 via-plug

24 mounting ball electrodes

31 ball electrode

41 interconnect pad

CELL I/O cell

CELL-A I/O cell on the outer position (outer periphery)

CELL-B I/O cell on the inner position (inner periphery)

CELL-1 first I/O cell

CELL-1A outer I/O cell

CELL-1B inner I/O cell

CELL-2 second I/O cell

CELL-2A outer I/O cell

CELL-2B inner I/O cell

PL peripheral

[Document Name] Abstract:

[Abstract]

[Problems] In a semiconductor device having a configuration in which ball electrodes mounted on a chip is connected to an interconnect pad on a packaging substrate, the miniaturization of a chip is intended while the increase of the number of terminals of ball electrodes is enabled. A method for fabricating the same is also provided.

[Solution] In this semiconductor device where a plurality of ball electrodes are arranged and formed on the chip, and the interconnect pads 21 to which the ball electrodes are connected is formed on the package substrate, a plurality of I/O cells CELL is configured where the interconnect pad 21 corresponding to the plurality of ball electrodes including at least the ball electrode for signal lines are grouped, and the I/O cells, as CELL-A and CELL-B, are arranged at positions the outer-periphery and the inner periphery of the chip. Even when the chip is miniaturized or the number of ball electrodes is increased, the drawing-out of the interconnect lines from the interconnect pad corresponding to each of the I/O cells .to the peripheral outer regions of the chip is possible, to realize the semiconductor device having the higher integration and the higher performances.

[Selected Drawing] Fig.3

FIG. 1

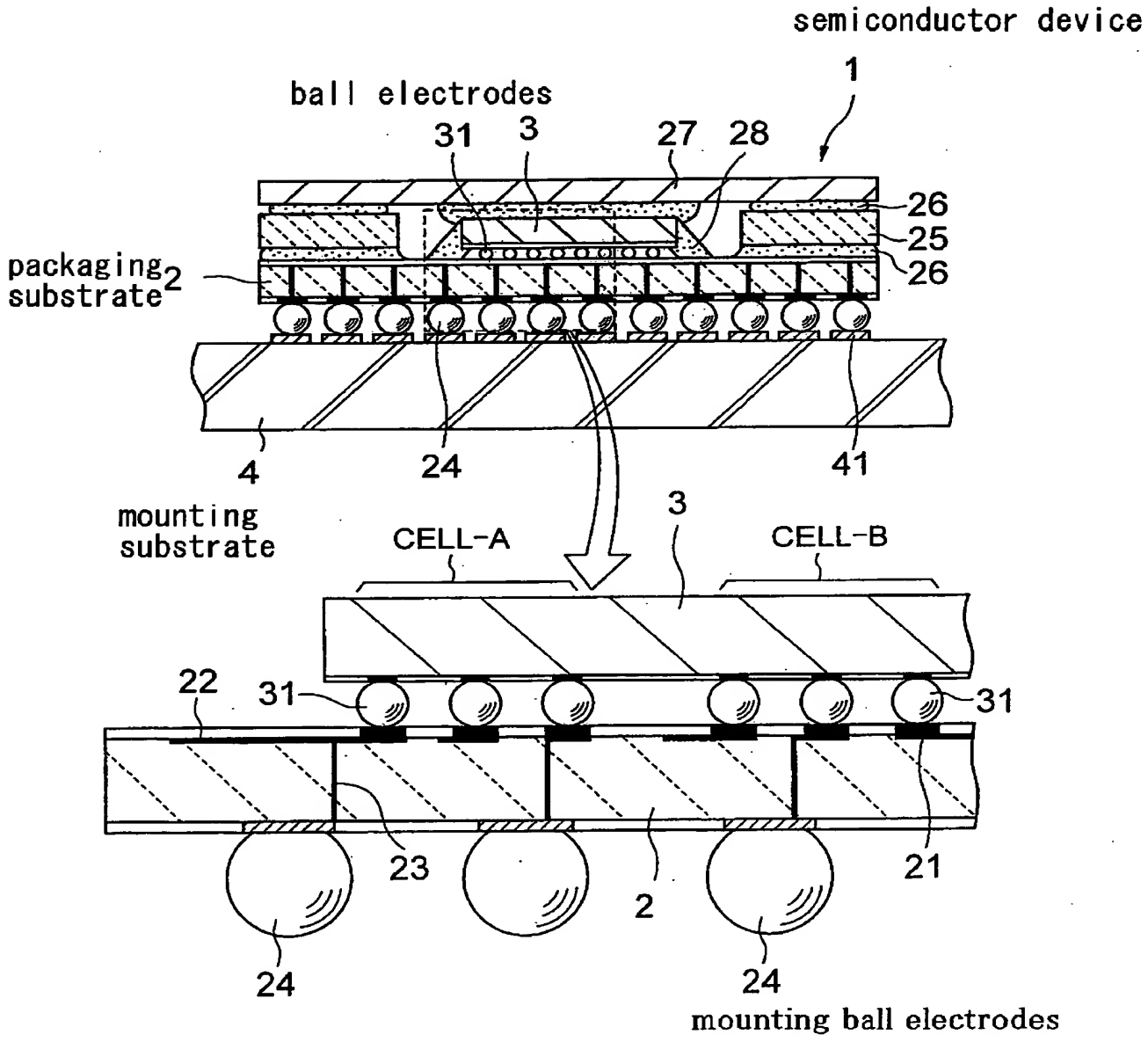

semiconductor device
1
ball electrodes
31
3
27
28
26
25
26
packaging substrate
2
4
24
41
mounting substrate
3
CELL-A
CELL-B
22
31
31
23
2
21
24
24
mounting ball electrodes

FIG. 2

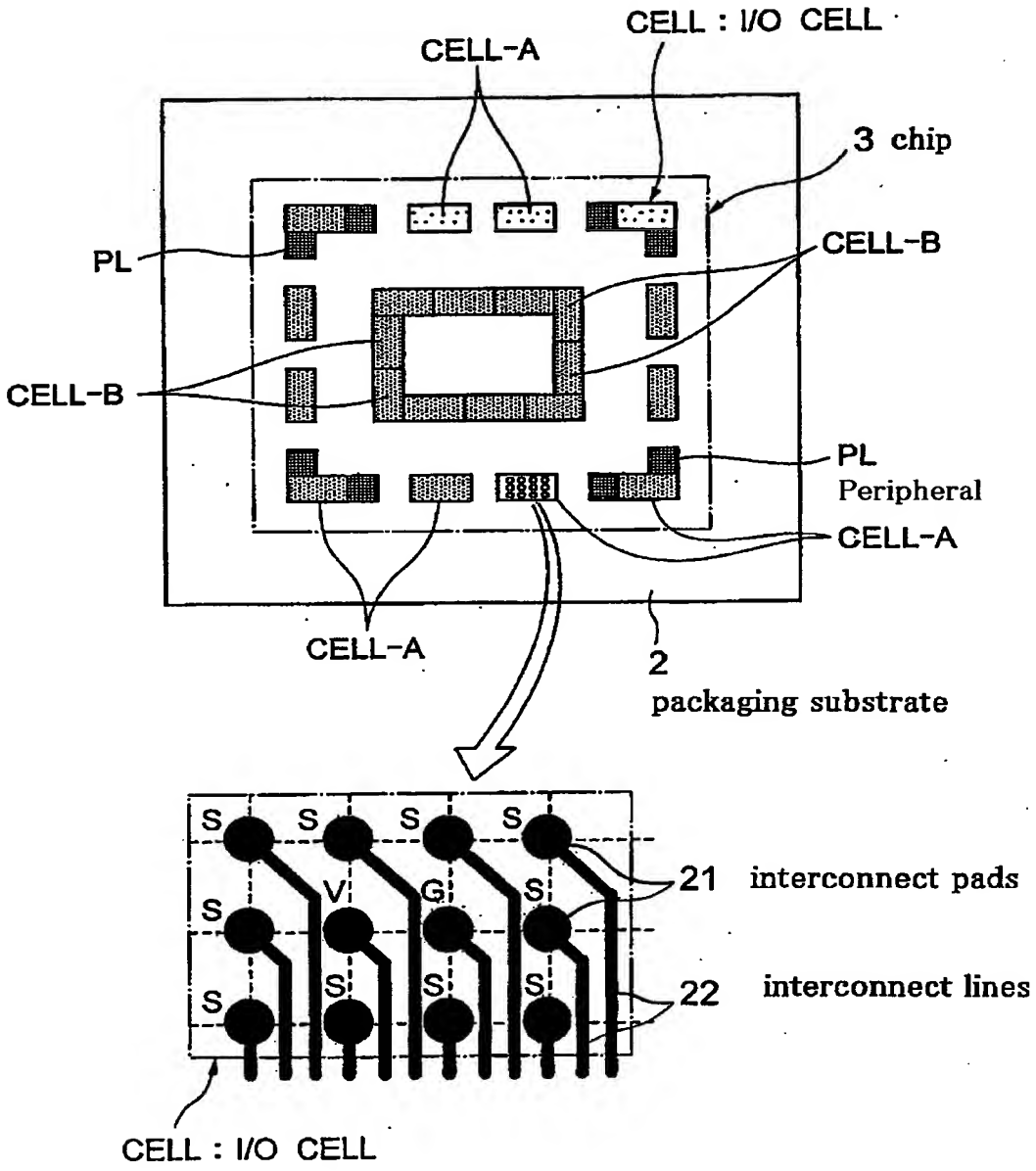

CELL : I/O CELL
CELL-A
3 chip
PL
CELL-B
CELL-B
PL
Peripheral
CELL-A
CELL-A
2
packaging substrate
S
V
G
21
interconnect pads
22
interconnect lines
CELL : I/O CELL

FIG. 3

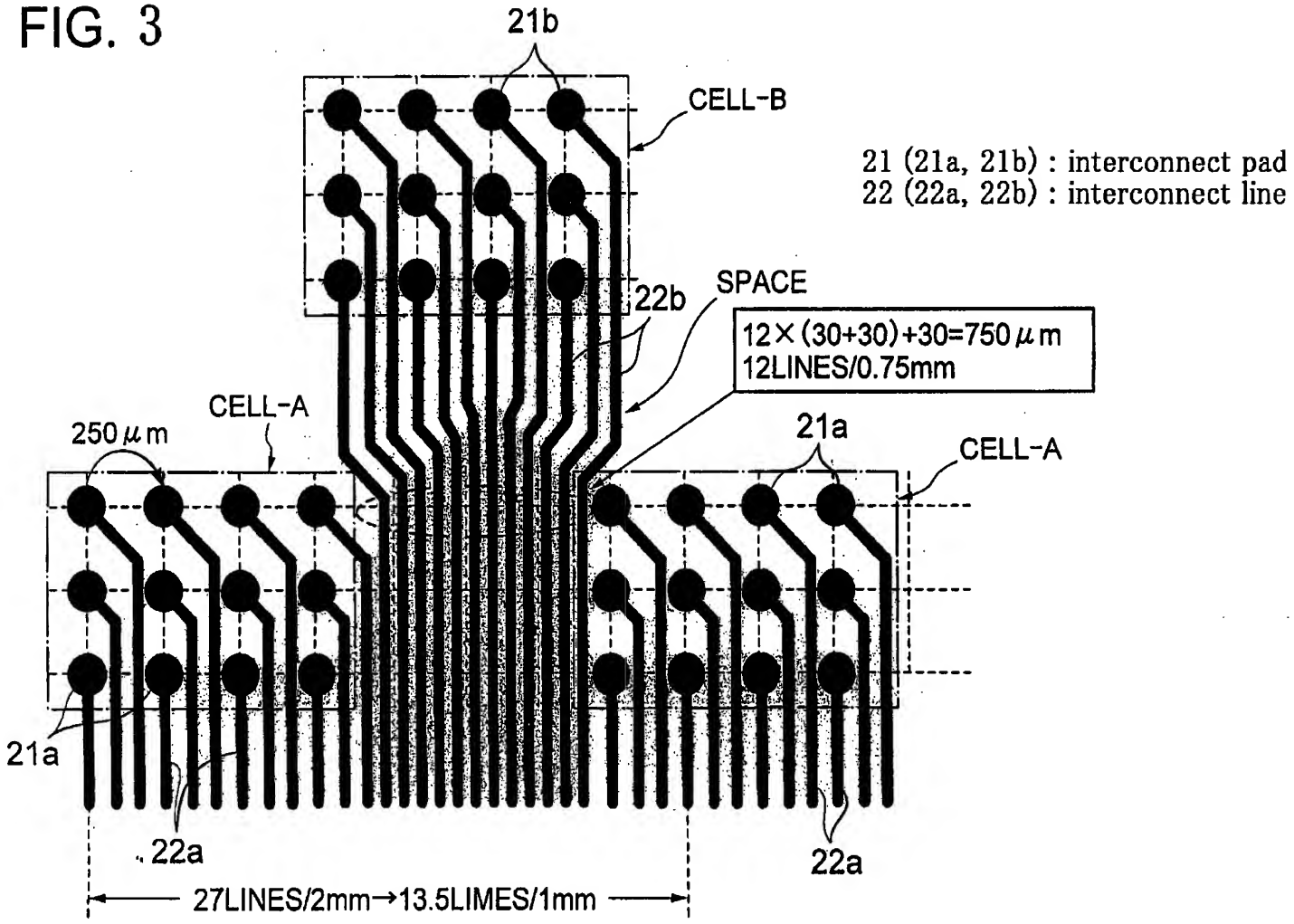

21b
CELL-B
21 (21a, 21b) : interconnect pad
22 (22a, 22b) : interconnect line
22b
SPACE
12×(30+30)+30=750μm
12LINES/0.75mm
CELL-A
250μm
21a
CELL-A
21a
22a
22a
27LINES/2mm→13.5LIMES/1mm

FIG. 4

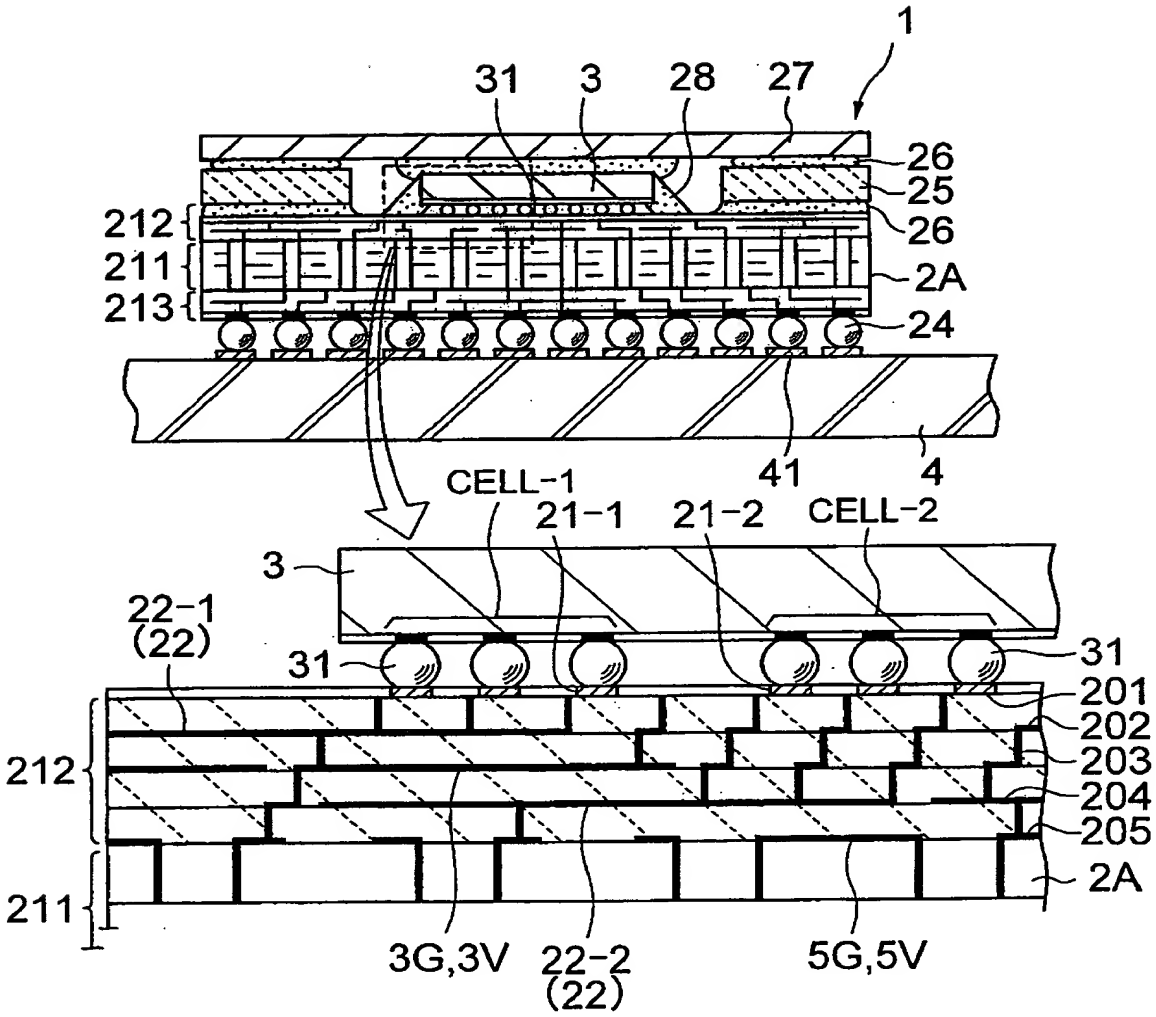

1
31
3
28
27
26
25
26
212
211
213
2A
24
41
4
CELL-1
21-1
21-2
CELL-2
3
22-1
(22)
31
31
201
202
203
204
205
2A
212
211
3G,3V
22-2
(22)
5G,5V

FIG. 5

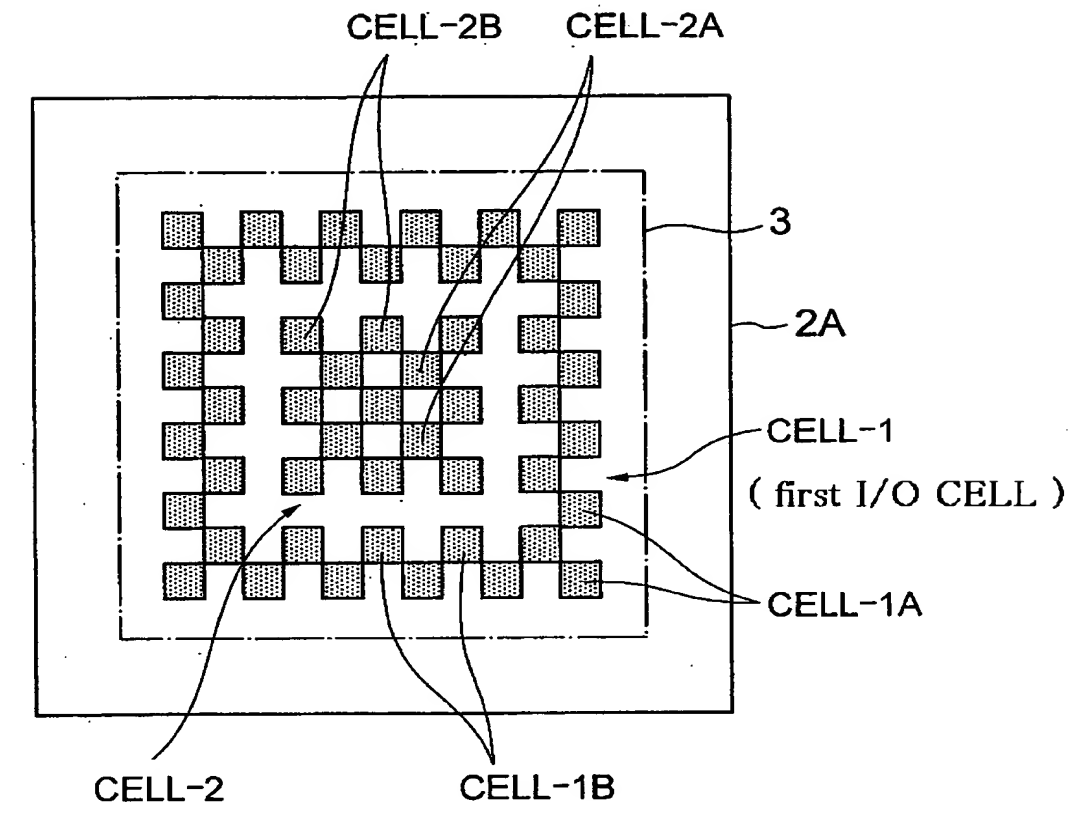

CELL-2B
CELL-2A
3
2A
CELL-1
(first I/O CELL)
CELL-1A
CELL-2
(second I/O CELL)
CELL-1B

FIG. 6

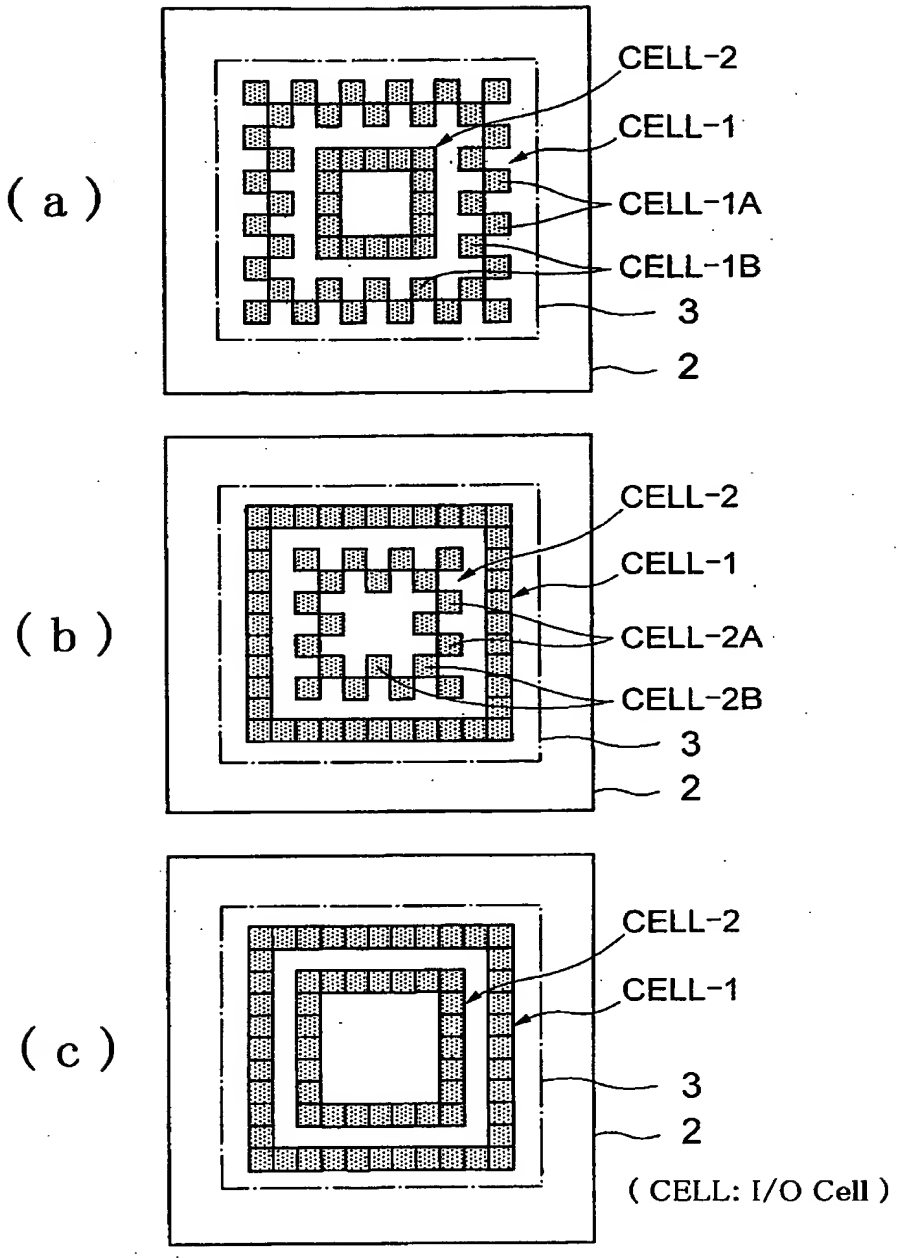
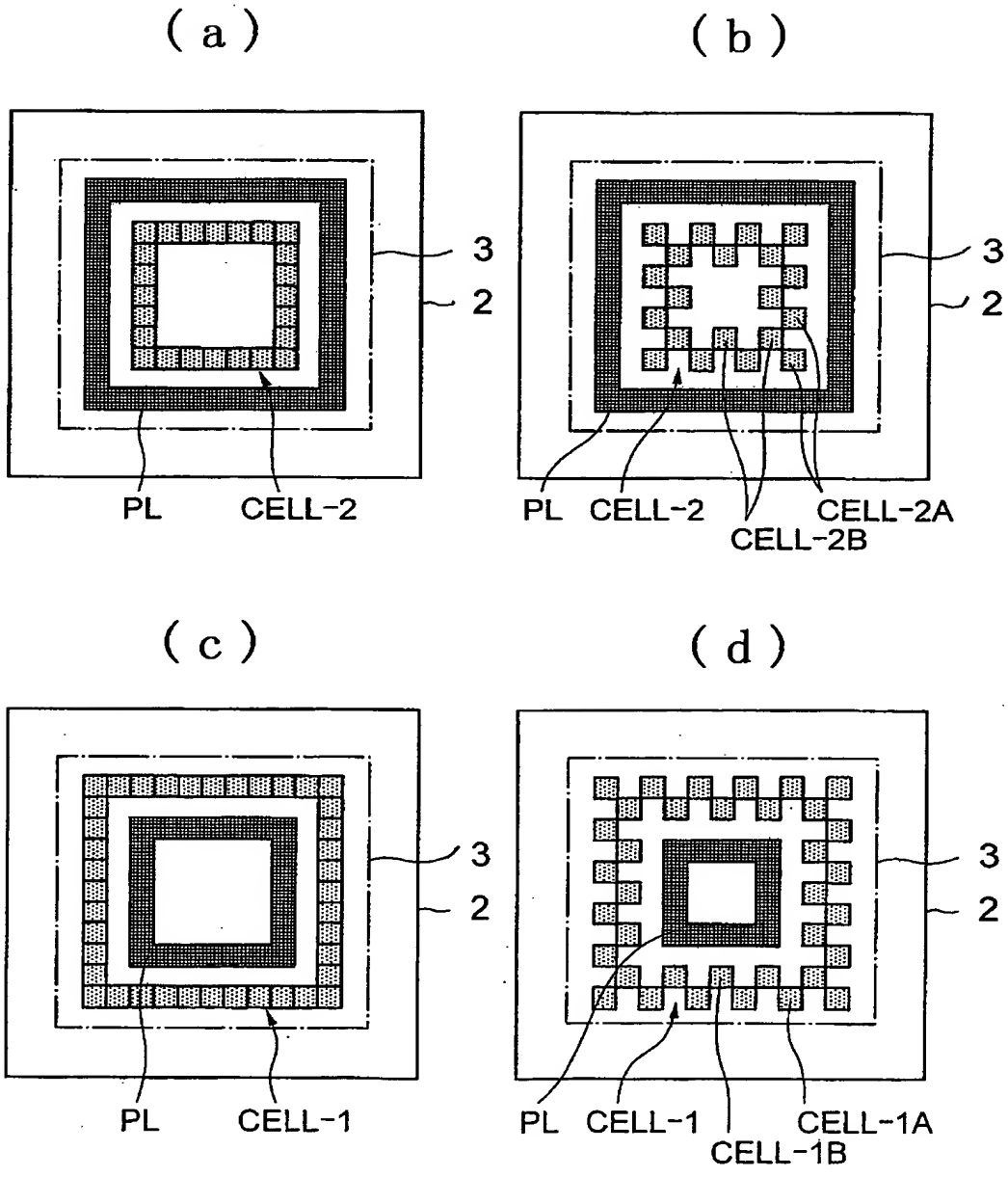
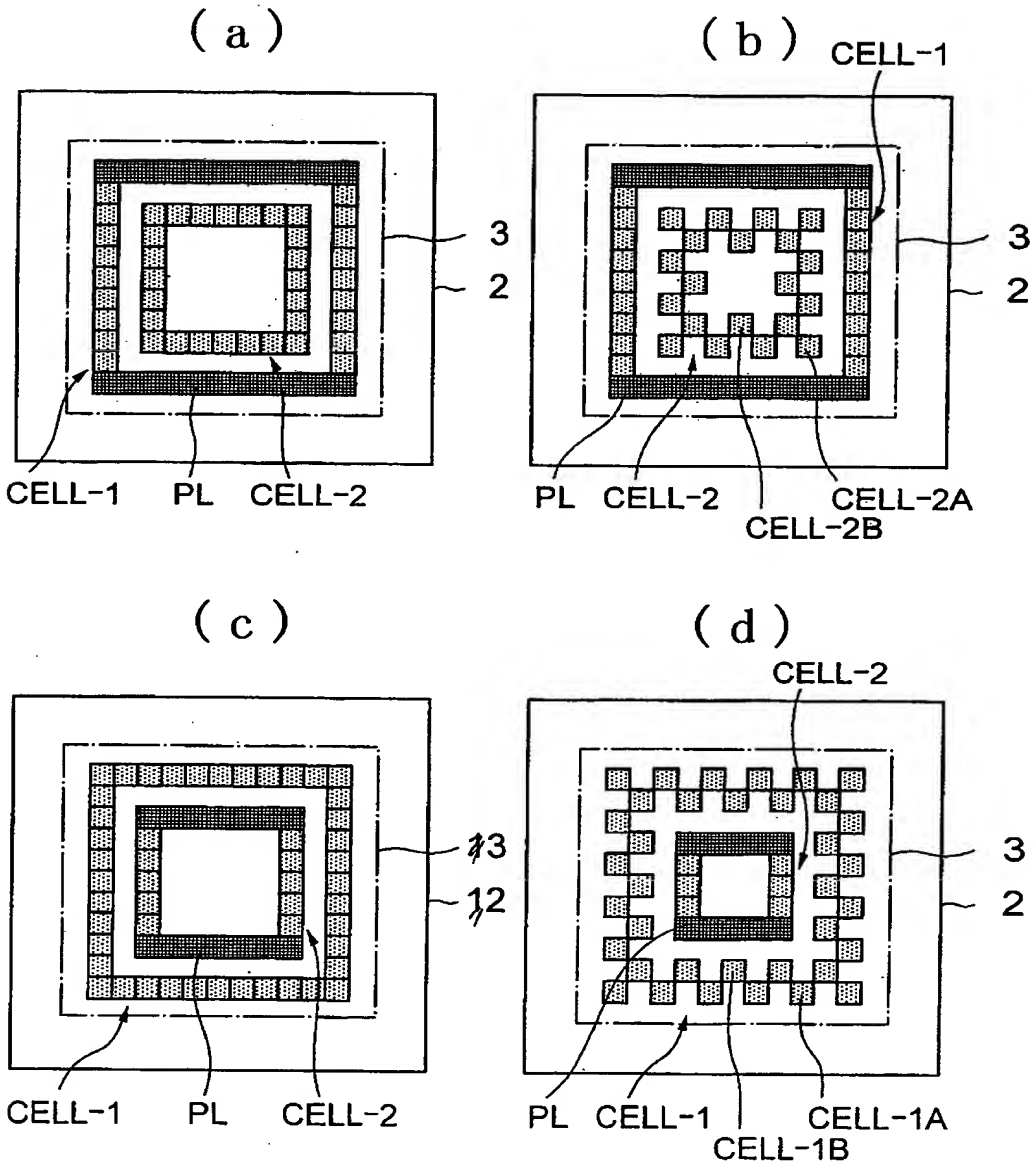

(a)
CELL-2
CELL-1
CELL-1A
CELL-1B
3
2
(b)
CELL-2
CELL-1
CELL-2A
CELL-2B
3
2
(c)
CELL-2
CELL-1
3
2
(CELL: I/O Cell)

FIG. 7



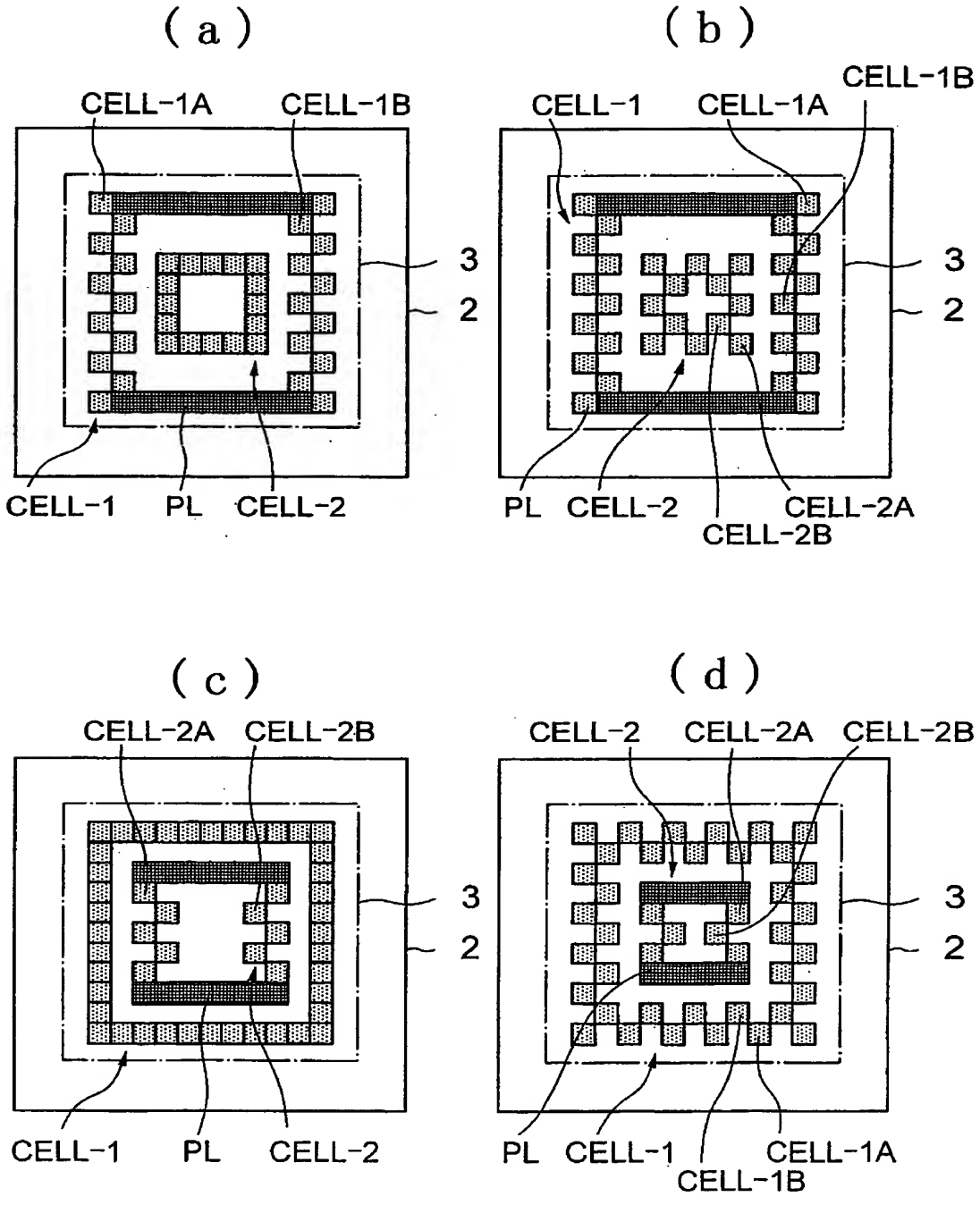
PL: Peripheral CELL: I/O Cell

FIG. 8



PL: Peripheral CELL: I/O Cell

FIG. 9



PL: Peripheral CELL: I/O Cell

FIG. 10

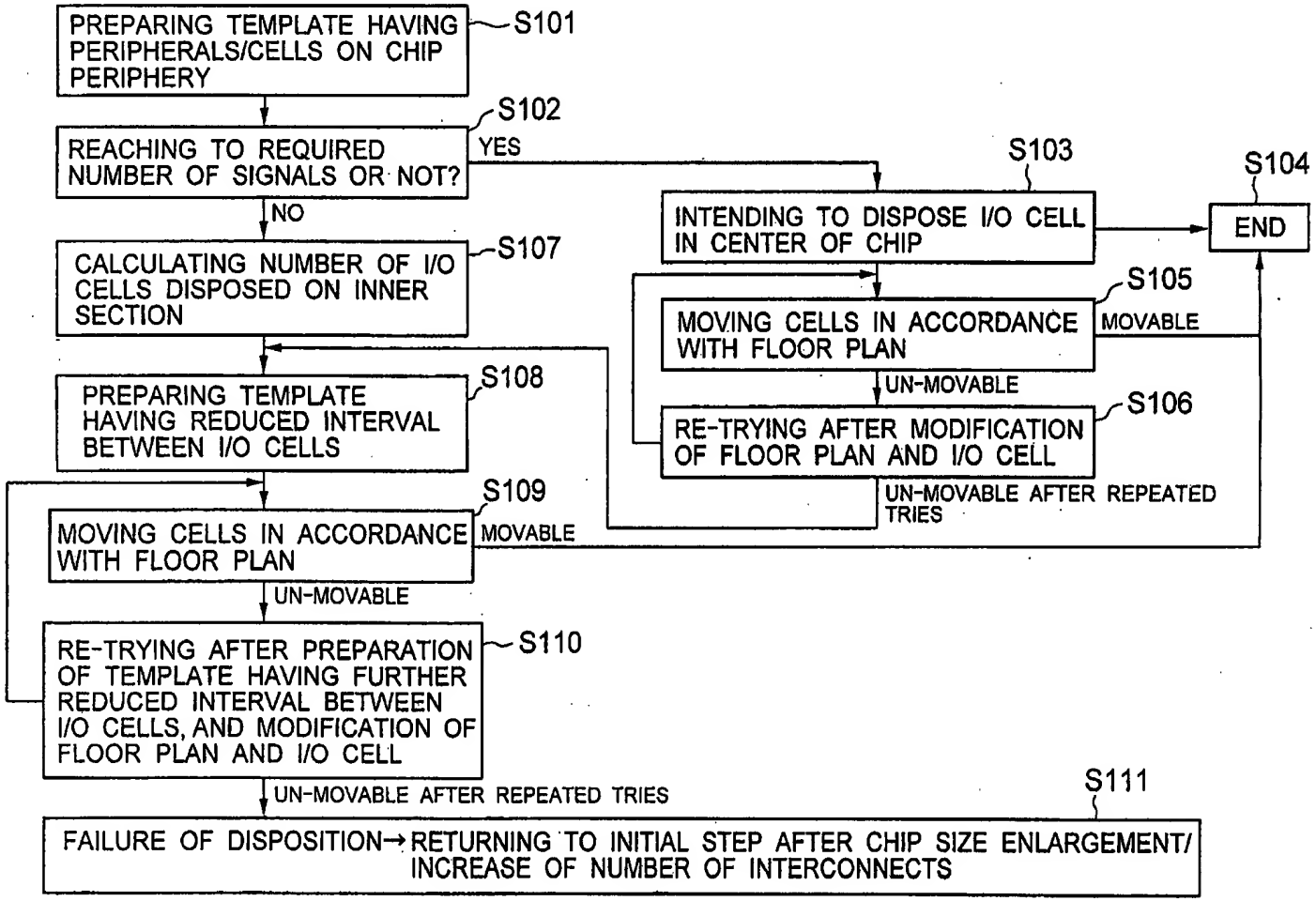

PREPARING TEMPLATE HAVING PERIPHERALS/CELLS ON CHIP PERIPHERY
S101
REACHING TO REQUIRED NUMBER OF SIGNALS OR NOT?
S102
YES
NO
INTENDING TO DISPOSE I/O CELL IN CENTER OF CHIP
S103
END
S104
CALCULATING NUMBER OF I/O CELLS DISPOSED ON INNER SECTION
S107
MOVING CELLS IN ACCORDANCE WITH FLOOR PLAN
S105
MOVABLE
UN-MOVABLE
RE-TRYING AFTER MODIFICATION OF FLOOR PLAN AND I/O CELL
S106
UN-MOVABLE AFTER REPEATED TRIES
PREPARING TEMPLATE HAVING REDUCED INTERVAL BETWEEN I/O CELLS
S108
MOVING CELLS IN ACCORDANCE WITH FLOOR PLAN
S109
MOVABLE
UN-MOVABLE
RE-TRYING AFTER PREPARATION OF TEMPLATE HAVING FURTHER REDUCED INTERVAL BETWEEN I/O CELLS, AND MODIFICATION OF FLOOR PLAN AND I/O CELL
S110
UN-MOVABLE AFTER REPEATED TRIES
S111
FAILURE OF DISPOSITION→RETURNING TO INITIAL STEP AFTER CHIP SIZE ENLARGEMENT/ INCREASE OF NUMBER OF INTERCONNECTS

FIG.11

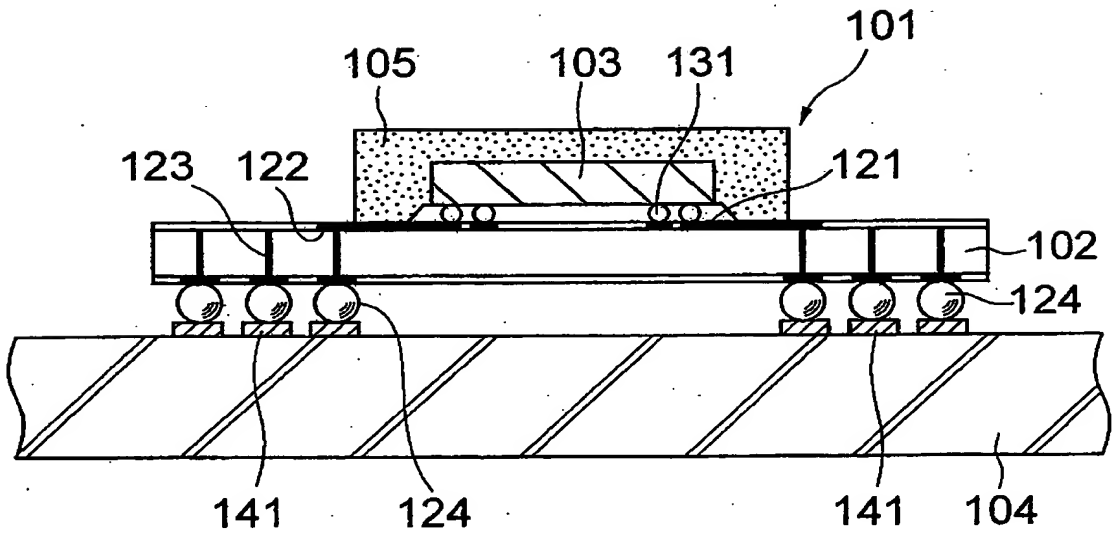


FIG.12

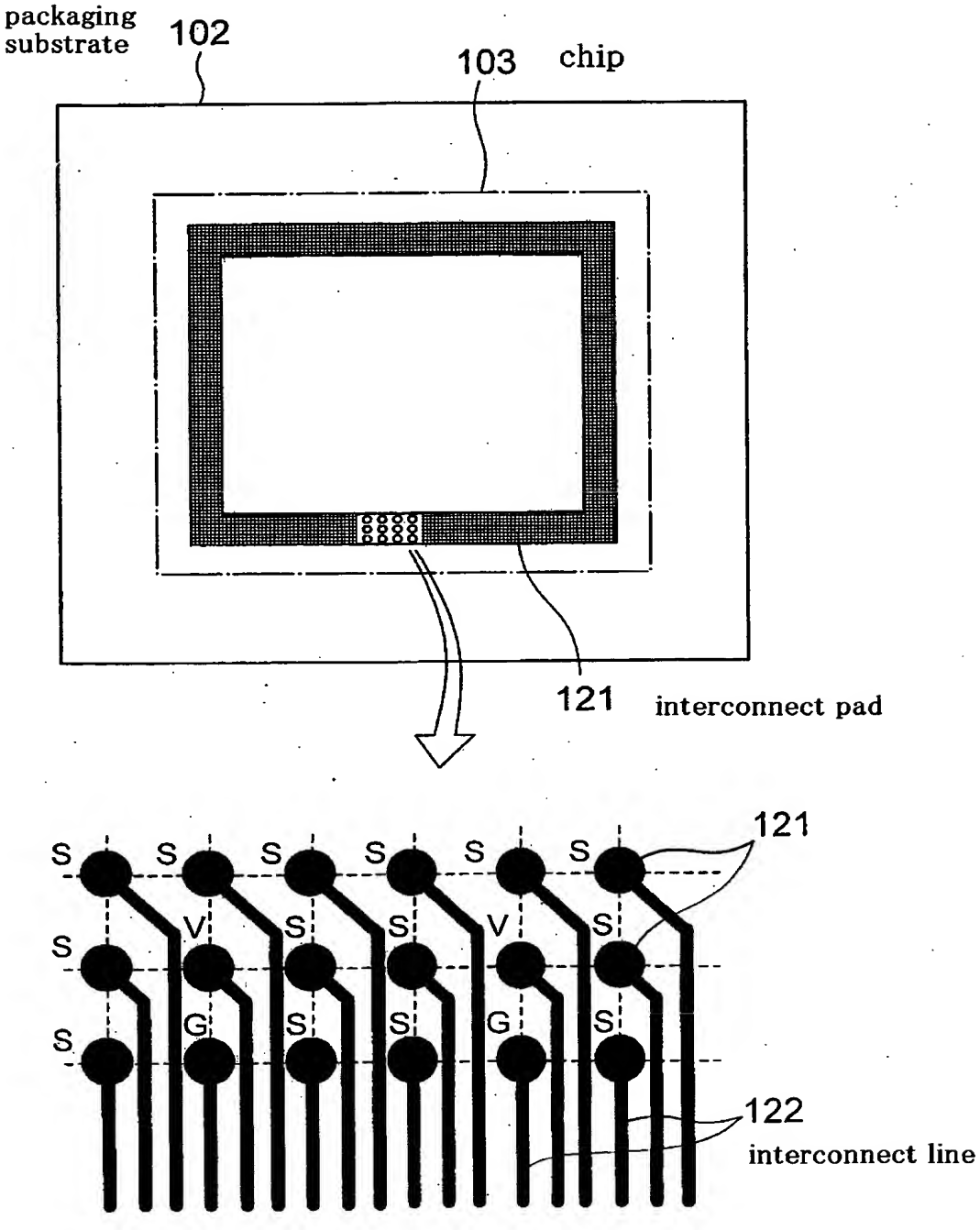

packaging substrate
102
103
chip
121
interconnect pad
121
S
V
G
122
interconnect line

FIG. 13